SOLID STATE IMAGE PICKUP DEVICE AND ITS CONTROL METHOD

This application is based on Japanese Patent Application HEI 11-161246, filed on June 8, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

a) Field of the Invention

The present invention relates to a solid state image pickup device having photoelectric conversion elements and its control method.

b) Description of the Related Art

Fig. 7 is a plan view of a general CCD type solid state image pickup device. The solid image pickup device is formed on a semiconductor substrate 1 made of silicon or the like and having a two-dimensional flat plane. The semiconductor substrate 1 has a plurality of photodiodes (photoelectric conversion elements) 2, vertical charge transfer paths (VCCD) 3, transfer gates (read gates) 4, a horizontal charge transfer path (HCCD) 6, and an output amplifier 7.

The photodiodes 2 are disposed in a two-dimensional matrix shape. Each photodiode converts received light into electric charges and stores the charges. Each vertical charge transfer path 3 is formed on the left side of each column of photodiodes 2 via transfer gates 4. The transfer gate 4 reads electric charges in the corresponding photodiode 2 to the vertical charge transfer path 3.

The vertical charge transfer path 3 is made of charge coupled devices (CCDs) and transfers electric charges read from the photodiodes 2 from the upper area of the drawing of Fig. 7 to the lower area (in a vertical direction). The horizontal charge transfer path 6 is made of CCDs, receives electric charges of one row unit

transferred from the vertical charge transfer paths 3 and transfers the charges from the left area of the drawing of Fig. 7 to the right area (in a horizontal direction).

The output amplifier 7 outputs a voltage corresponding to the amount of electric charges transferred from the horizontal charge transfer path 6. This voltage value corresponds to a pixel value. Each photodiode 2 corresponds to a pixel. By disposing the photodiodes 2 two-dimensionally, signals of a two-dimensional image can be obtained.

The number of pixels of a solid state image pickup device of a recent digital camera is increasing greatly in order to improve the image quality. Digital cameras having a solid state image pickup device having a number of pixels, one million pixels or larger generally called mega pixels, are being developed. As the number of pixels of a solid state image pickup device increases, a time taken to read image signals of one frame prolongs essentially. Although a prolonged read time of image signals does not become a fatal problem in reproducing a still image, a moving image is associated with a problem that the image signal read time cannot follow the frame rate (generally 1/30 sec for NTSC signals).

As the number of pixels exceeds one million, it is difficult to read moving images at the frame rate of 1/30 sec. Therefore, a solid state image pickup device of a mega pixel order does not reproduce moving images obtained by all pixels on a display, but reduces the data amount (pixel number) to reproduce moving images so as to follow the frame rate.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solid state image pickup device and its control method capable of reducing the image data amount without lowering a sensitivity or color balance.

According to one aspect of the present invention, there is provided a solid state image pickup device comprising: a plurality of photoelectric conversion elements for converting light into electric charges, the photoelectric conversion elements being uniformly disposed on a two-dimensional plane in vertical and horizontal directions; a plurality of vertical charge transfer paths for transferring electric charges to a downstream side in the vertical direction, the vertical charge transfer path being disposed adjacent to vertically and uniformly disposed photoelectric conversion elements; a read gate for reading electric charges from each photoelectric conversion element to the adjacent vertical charge transfer path; vertical addition means for adding electric charges of two or more photoelectric conversion elements on the vertical charge transfer path, by controlling the read gates and the vertical charge transfer path to read electric charges from some of the plurality of photoelectric conversion elements to the vertical charge transfer path, transfer the read electric charges on the vertical charge transfer path to the downstream side in the vertical direction, and read electric charges from others of the plurality of photoelectric elements on the downstream side to the vertical charge transfer path; a horizontal charge transfer path for transferring electric charges to a downstream side in the horizontal direction, the horizontal charge transfer path being disposed adjacent to one ends of the plurality of vertical charge transfer paths; a transfer gate for transferring electric charges on the vertical charge transfer paths to the horizontal charge transfer path; and horizontal addition means for adding electric charges transferred from two or more of the vertical charge transfer paths, on the horizontal charge transfer path, by controlling the transfer gate and the horizontal charge transfer path to transfer electric charges from some of the plurality of vertical charge transfer paths to the horizontal charge transfer path, transfer the electric charges on the horizontal charge transfer path to the downstream side in the horizontal direction,

and transfer electric charges from others of the plurality of vertical charge transfer paths on the downstream side to the horizontal charge transfer path.

According to another aspect of the present invention, there is provided a control method for a solid state image pickup device having a plurality of photoelectric conversion elements for converting light into electric charges, the photoelectric conversion elements being uniformly disposed on a two-dimensional plane in vertical and horizontal directions, a plurality of vertical charge transfer paths for transferring electric charges to a downstream side in the vertical direction, the vertical charge transfer path being disposed adjacent to vertically and uniformly disposed photoelectric conversion elements, a horizontal charge transfer path for transferring electric charges to a downstream side in the horizontal direction, the horizontal charge transfer path being disposed adjacent to one ends of the plurality of vertical charge transfer paths, the method comprising the steps of: (a) reading electric charges from some of the plurality of photoelectric conversion elements to the vertical charge transfer path; (b) transferring the electric charges on the vertical charge transfer path to a downstream side in the vertical direction; (c) reading electric charges from others of the plurality of photoelectric conversion elements on the downstream side to the vertical charge transfer path and adding the read electric charges to the electric charges transferred to the downstream side; (d) transferring electric charges from some of the plurality of vertical charge transfer paths to the horizontal charge transfer path;(e) transferring the electric charges on the horizontal charge transfer path to a downstream side in the horizontal direction; and (f) transferring electric charges from others of the plurality of vertical charge transfer paths on the downstream side to the horizontal charge transfer path and adding electric charges from two or more vertical charge transfer paths on the horizontal charge transfer path.

The vertical charge transfer path adds electric charges of two or more photoelectric conversion elements, and the horizontal charge transfer path also adds electric charges transferred from two or more vertical charge transfer paths. Since electric charges of four or more photoelectric conversion elements in total, can be added together, the image data amount can be reduced.

Electric charges of photosensitive conversion elements not only in the vertical direction but also in the horizontal direction are added for pixel mixing. It is therefore possible to reduce the pixel data amount, improve a sensitivity, and obtain reduced image data having a good color balance.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a partial plan view of a color solid state image pickup device according to an embodiment of the invention, and Figs. 1B to 1F are timing charts illustrating a transfer and addition operation of signal charges on a horizontal charge transfer path.

Figs. 2A to 2C are schematic plan views illustrating a read and addition operation of signal charges on a vertical charge transfer path of a color solid state image pickup device according to an embodiment of the invention.

Fig. 3 is a plan view showing the structure of control electrodes of a color solid state image pickup device according to an embodiment of the invention.

Fig. 4A to 4C are cross sectional views showing the structure of the control electrodes of the color solid state image pickup device of the embodiment.

Fig. 5 is a plan view showing the structure of control electrodes of a color solid state image pickup device according to another embodiment of the invention.

Fig. 6A and 6B are cross sectional views showing the structure of the

control electrodes of the color solid state image pickup device of the embodiment.

Fig. 7 is a plan view showing the fundamental structure of a solid state image pickup device.

Fig. 8 is a plan view showing the structure of control electrodes of a color solid state image pickup device according to another embodiment of the invention.

Figs. 9A to 9E are a cross sectional view taken along line 1X-1X' of Fig. 8 and potential diagrams.

Figs. 10A to 10E are a cross sectional view taken along line X-X' of Fig. 8 and potential diagrams.

Figs. 11A to 11D are a cross sectional view taken along line X-X' of Fig. 8 and potential diagrams.

Fig. 12 is a partial plan view of a color solid state image pickup device of a honeycomb structure according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1A is a partial plan view showing a color solid state image pickup device according to an embodiment of the invention, and Figs. 1B to 1F are timing charts illustrating a transfer and addition operation of signal charges on a horizontal charge transfer path 6. The fundamental structure of the solid state image pickup device of this embodiment is similar to that shown in Fig. 7, including photodiodes 2, vertical charge transfer paths 3-1 to 3-6, transfer gates 4, a horizontal charge transfer path 6 and an output amplifier 7. A control unit 8 controls the solid state image pickup device.

Control electrodes 5 control the read (transfer) operation of electric charges from the vertical charge transfer paths 3-1 to 3-6 to the horizontal charge

transfer path 6. First transfer electrodes 6b indicated by broken lines are formed over the horizontal charge transfer path 6 via an insulating film, and second transfer electrodes 6a indicated by solid lines are formed over the first transfer electrodes 6b via another insulating film. By applying two-phase transfer pulses to the electrodes 6a and 6b, electric charges are transferred along the horizontal charge transfer path 6 from left to right (in a horizontal direction).

A color filter layout of photodiodes (pixels) 2 shown in Fig. 1A is the Bayer matrix. R represents a red pixel, G represents a green pixel, and B represents a blue pixel. Each of the vertical charge transfer paths 3-1 to 3-6 or all of them are called, where applicable, simply a vertical charge transfer path 3.

A method of reducing a data amount through addition of pixel values in a vertical direction will be described with reference to Figs. 2A to 2C showing one vertical charge transfer path 3-1. As shown in Fig. 2A, electric charges are read from an R pixel photodiode 21, from a G pixel photodiode 22 at the next lower row, from an R pixel photodiode 25 at the third lower row, and from a G pixel photodiode 26 at the next lower row. Namely, electric charges are read from a pair of upper and lower adjacent R and G photodiodes and from a pair of upper and lower adjacent R and G photodiodes spaced by two rows from the first pair, via transfer gates 4 to the vertical charge transfer path 3-1.

Next, as shown in Fig. 2B, the electric charges R and G on the vertical charge transfer path 3-1 are transferred downwards by one row. Then, as shown in Fig. 2C, the electric charges are transferred further downwards by one row. At this timing shown in Fig. 2C, electric charges not read at the timing shown in Fig. 2A are read from an R pixel photodiode 23, from a G pixel photodiode 24 at the next lower row, from an R pixel photodiode 27 at the third lower row, and from a G pixel photodiode 28 at the next lower row, respectively to the vertical charge transfer path

3-1. Namely, electric charges are read from a pair of upper and lower adjacent R and G photodiodes and from a pair of upper and lower adjacent R and G photodiodes spaced by two rows from the first pair, via transfer gates 4 to the vertical charge transfer path 3-1.

Therefore, the electric charges R and G transferred from the upper rows are added to (mixed with) the electric charges R and G on the vertical charge transfer path 3-1. The added charges are represented by RR and GG. Electric charges for blue pixels are added in a similar manner and are represented by BB as shown in Fig. 1A. Two pixels adjacent in the vertical direction for each color are added and the number of pixels in the vertical direction is halved.

By repeating the charge read and transfer operation in the vertical direction, electric charges of two pixels (photodiodes) of the same color separated by two rows in the vertical direction are added together, and transferred on the vertical charge transfer path 3 as vertically added two-pixel electric charges RR, GG and BB. This means that the pixel data amount is halved substantially in the vertical direction.

Next, the operation of adding the vertically added two-pixel electric charges also in the horizontal direction to further reduce the pixel data amount will be described with reference to Figs. 1B to 1F.

Figs. 1B to 1F time sequentially illustrate the charge transfer on the horizontal charge transfer path 6.

At the timing shown in Fig. 1B, the vertically added two-pixel electric charges GG and BB on the vertical charge transfer paths 3-1 to 3-6 at the lowest row are read to the horizontal charge transfer path 6. At this timing, as shown in Fig. 1B, although the vertically added two-pixel electric charges GG and BB are read from the vertical charge transfer paths 3-1, 3-2, 3-5 and 3-6, the vertically added two-pixel electric charges GG and BB are not read from the vertical charge transfer paths 3-3

and 3-4 between the vertical charge transfer paths 3-1, 3-2, 3-5 and 3-6.

More specifically, electric charges are read from a pair of two columns of the vertical charge transfer paths 3 and a pair of two columns spaced by two columns from the first pair. This selective read is controlled by the control electrodes 5. The details of the control electrodes 5 will be given later with reference to Fig. 3 and Figs. 4A to 4C.

Next, the vertically added two-pixel electric charges GG and BB read at the timing shown in Fig. 1B are transferred by two columns (two vertical charge transfer paths) in the horizontal direction. At this timing, the vertically added two-pixel electric charges GG and BB on the vertical charge transfer paths 3-3 and 3-4 at the lowest row not read at the timing shown in Fig. 1B are read to the horizontal charge transfer path 6. Therefore, as shown in Fig. 1C, the vertically added two-pixel electric charges GG and BB transferred in the horizontal direction are added to the vertically added two-pixel electric charges GG and BB read from the vertical charge transfer paths 3-3 and 3-4 to become GGGG and BBBB. In this manner, pixels of two pairs of two columns in the horizontal direction are added, i.e., four pixels are added.

Next, electric charges on the vertical charge transfer paths 3-1 to 3-6 are transferred downwards by one row in the vertical direction, so that vertically added two-pixel electric charges RR and GG are positioned at the lowest row of the vertical charge transfer paths. Thereafter, as shown in Fig. 1D, the vertically added two-pixel electric charges RR and GG are read from the vertical charge transfer paths 3-1, 3-2, 3-5 and 3-6 to the horizontal charge transfer path 6.

Next, the electric charges on the horizontal charge transfer path 6 are transferred by two columns in the horizontal direction, as shown in Fig. 1E.

Electric charges on the vertical charge transfer paths 3-3 and 3-4 not

read at the timing shown in Fig. 1D are transferred downwards in the vertical direction, so that vertically added two-pixel electric charges RR and GG are positioned at the lowest row of the vertical charge transfer paths. The vertically added two-pixel electric charges RR and GG on the vertical charge transfer paths 3-3 and 3-4 at the lowest row are read to the horizontal charge transfer path 6. Therefore, as shown in Fig. 1F, the vertically added two-pixel electric charges RR and GG transferred in the horizontal direction are added to the vertically added two-pixel electric charges RR and GG read from the vertical charge transfer paths 3-3 and 3-4 to become RRRR and GGGG.

As shown in Fig. 1F, the added electric charges of four pixels for each color disposed efficiently on the horizontal charge transfer path 6 are transferred right in the horizontal direction, and the output amplifier 7 outputs pixel signals of substantially four rows. Thereafter, the above-described operations are repeated to output pixel signals of one frame.

This means that the pixel data amount is substantially halved both in the vertical and horizontal directions and the total pixel data amount is reduced by 1/4. Since data of a plurality of pixels is added, the sensitivity can be improved substantially. As compared to reducing the pixel data amount by thinning pixel data, the information amount is larger and the image quality can be improved more.

In the embodiment described with reference to Figs. 1A to 1F and Figs. 2A to 2C, electric charges are added for two rows in the vertical direction and two columns in the horizontal direction. The numbers of rows and columns in the vertical and horizontal directions are not limited only to two, but three or more rows and columns may be used in the vertical and horizontal directions to further reduce the data amount. In this case, a similar method described above can be used basically by changing the read timings.

The selective read of electric charges from the vertical charge transfer paths 3-1 to 3-6 to the horizontal charge transfer path 6 can be controlled by the control electrodes 5. Fig. 3 is a plan view showing an example of the structure of control electrodes 5 used for addition of electric charges of three columns in the horizontal direction.

Fig. 4A is a cross sectional view taken along line I-I' of Fig. 3, Fig. 4B is a cross sectional view taken along line II-II' of Fig. 3, and Fig. 4C is a cross sectional view taken along line III-III' of Fig. 3.

Referring to Fig. 3, H_{6n}, H_{6n+1}, H_{6n+2}, H_{6n+3}, H_{6n+4}, and H_{6n+5} represent a vertical charge transfer path (n-type semiconductor region in a p-type semiconductor region 11 shown in Figs. 4A to 4C), and reference numeral 6 represents a horizontal charge transfer path. First polysilicon layer electrodes V_{c1} and V_{c4} indicated by broken lines are formed over the vertical charge transfer paths via an insulating film (SiO_2) 12, and second polysilicon layer electrodes V_{c2}, V_{c3} and V_{c5} indicated by solid lines are formed over the first polysilicon layer electrodes V_{c1} and V_{c4} via an insulating film (SiO_2) 13. These five electrodes V_{c1} to V_{c5} constitute the control electrodes 5. A transfer control signal of either a high or low level is supplied from the control unit 8 (Fig. 1A) to these control electrodes to select the vertical charge transfer paths H_{6n}, H_{6n+1}, H_{6n+2}, H_{6n+3}, H_{6n+4}, and H_{6n+5} and read (transfer) electric charges from the selected vertical charge transfer paths to the horizontal charge transfer path 6. One unit of the vertical charge transfer paths H_{6n}, H_{6n+1}, H_{6n+2}, H_{6n+3}, H_{6n+4}, and H_{6n+5} is disposed repetitively along the horizontal direction in Fig. 3.

Fig. 4A is a cross sectional view showing the control electrodes along the vertical charge transfer path H_{6n}. The electrodes V_{c1}, V_{c3} and V_{c4} are disposed on the insulating film 12 over the vertical charge transfer path H_{6n}, in this order sequentially from the upper area to lower area (downwards in the vertical direction) in

Fig. 3. The structures of the vertical charge transfer path H_{6n+1} and control electrodes over this path have the same structures as the vertical charge transfer path H_{6n} and control electrodes over this path. The electrode V_{c5} is disposed on the insulating film 13 over the electrode V_{c4}.

Fig. 4B is a cross sectional view showing the control electrodes along the vertical charge transfer path H_{6n+2}. The electrodes V_{c1}, V_{c2} and V_{c4} are disposed on the insulating film 12 over the vertical charge transfer path H_{6n+2}, in this order sequentially from the upper area to lower area (downwards in the vertical direction) in Fig. 3. The structures of the vertical charge transfer path H_{6n+3} and control electrodes over this path have the same structures as the vertical charge transfer path H_{6n+2} and control electrodes over this path. The electrodes V_{c3} and V_{c5} are disposed on the insulating film 13 over the electrode V_{c4}.

Fig. 4C is a cross sectional view showing the control electrodes along the vertical charge transfer path H_{6n+4}. The electrodes V_{c1}, V_{c2}, V_{c4}, V_{c3} and V_{c5} are disposed on the insulating film 12 over the vertical charge transfer path H_{6n+4}, in this order sequentially from the upper area to lower area (downwards in the vertical direction) in Fig. 3. The structures of the vertical charge transfer path H_{6n+5} and control electrodes over this path have the same structures as the vertical charge transfer path H_{6n+4} and control electrodes over this path. The electrode V_{c3} is disposed on the insulating film 13 over the electrode V_{c4}.

For addition of electric charges of two columns in the horizontal direction described with Fig. 1A, one unit of vertical charge transfer paths H_{6n}, H_{6n+1}, H_{6n+2} and H_{6n+3} is disposed repetitively in the horizontal direction in Fig. 3.

Addition of electric charges of two columns in the horizontal direction will be described with reference to Fig. 5 and Figs. 6A and 6B.

Fig. 5 is a plan view showing an example of the structure of control

electrodes 5 used for addition of electric charges of two columns in the horizontal direction.

Fig. 6A is a cross sectional view taken along line IV-IV' of Fig. 5, and Fig. 6B is a cross sectional view taken along line V-V' of Fig. 5.

Referring to Fig. 5, H_{4m}, H_{4m+1}, H_{4m+2} and H_{4m+3} represent a vertical charge transfer path (n-type semiconductor region in a p-type semiconductor region 11 shown in Figs. 6A and 6B), and reference numeral 6 represents a horizontal charge transfer path. First polysilicon layer electrodes V_{c11} and V_{c14} indicated by broken lines are formed over the vertical charge transfer paths via an insulating film (SiO_2) 12, and second polysilicon layer electrodes V_{c12}, V_{c13} and V_{c15} indicated by solid lines are formed over the first polysilicon layer electrodes V_{c11} and V_{c14} via an insulating film (SiO_2) 13. These five electrodes V_{c11} to V_{c15} constitute the control electrodes 5. A transfer control signal of either a high or low level is supplied from the control unit 8 (Fig. 1A) to these control electrodes to select the vertical charge transfer paths H_{4m}, H_{4m+1}, H_{4m+2}, and H_{4m+3} and read (transfer) electric charges from the selected vertical charge transfer paths to the horizontal charge transfer path 6. One unit of the vertical charge transfer paths H_{4m}, H_{4m+1}, H_{4m+2} and H_{4m+3} is disposed repetitively along the horizontal direction in Fig. 5.

Fig. 6A is a cross sectional view showing the control electrodes along the vertical charge transfer path H_{4m}. The electrodes V_{c11}, V_{c13} and V_{c14} are disposed on the insulating film 12 over the vertical charge transfer path H_{4m}, in this order sequentially from the upper area to lower area (downwards in the vertical direction) in Fig. 5. The structures of the vertical charge transfer path H_{4m+1} and control electrodes over this path have the same structures as the vertical charge transfer path H_{4m} and control electrodes over this path.

Fig. 6B is a cross sectional view showing the control electrodes along

the vertical charge transfer path H_{4m+2}. The electrodes V_{c11}, V_{c12}, V_{c14} and V_{c15} are disposed on the insulating film 12 over the vertical charge transfer path H_{4m+2}, in this order sequentially from the upper area to lower area (downwards in the vertical direction) in Fig. 5. The structures of the vertical charge transfer path H_{4m+3} and control electrodes over this path have the same structures as the vertical charge transfer path H_{4m+2} and control electrodes over this path.

Fig. 8 is a plan view showing another example of the structure of control electrodes 5 shown in Fig. 1A. Figs. 9A to 9E are cross sectional views taken along lines IX-IX' of Fig. 8. Figs. 10A to 10E are cross sectional views taken along line X-X' of Fig. 8. Electrodes 31 to 34 correspond to the control electrodes.

As shown in Figs. 9A and 10A, vertical charge transfer paths 3-1 to 3-4 and a horizontal charge transfer path 6 are made of n-type semiconductor regions in a p-type semiconductor region 41. First polysilicon (electrode) layers 31, 33 and 35a are formed on an insulating film 43 over semiconductor regions 3 and 6.

In the vertical charge transfer paths 3-1 and 3-2, p-type impurity ions such as B are implanted into a semiconductor region 36a under an area between the first polysilicon layers 31 and 33. The p-type region 36a can be formed by self-alignment ion implantation using the first polysilicon layers 31 and 33 as a mask.

In all the vertical charge transfer paths 3-1 to 3-4, p-type impurity ions are implanted into a semiconductor region 37 under an area between the first polysilicon layers 33 and 35a. The p-type region 37 can be formed by self-alignment ion implantation using the first polysilicon layers 33 and 35a as a mask.

Thereafter, second polysilicon (electrode) layers 32, 34 and 35b are formed on an insulating film 43 over the semiconductor regions 36 and 37 and first polysilicon layers 31, 33 and 35a.

A signal ST is applied to the electrode 31, a signal C1 is applied to the

electrodes 32 and 33, a signal C2 is applied to the electrode 34. Two-phase drive pulses φ1 and φ2 are applied to the electrodes 35a and 35b. In the horizontal charge transfer path 6, the semiconductor region under the electrode 35a is an n-type well region, and the semiconductor region under the electrode 35b is a p-type barrier region (or low concentration n-type barrier layer).

A method of transferring the charges only in the vertical charge transfer paths 3-1 and 3-2 to the horizontal charge transfer path 6 and maintaining the charges on the vertical charge transfer paths 3-3 and 3-4 will be described.

In Figs. 9A and 10A, the signal ST is set to a positive potential, the signal C1 is set to 0 V, the signal C2 is set to 0 V, and the signal φ1 is set to 0V. As shown in Figs. 9B and 10B, the potentials at the semiconductor regions under the electrodes 31, 32, 33, 34 and 35a therefore become P1, P2, P3, P4 and P5.

The vertical charge transfer path 3-1 shown in Fig. 9A has the p-type region 36a. Therefore, the potential P2 at the vertical charge transfer path 3-1 becomes higher than the potential P2 at the vertical charge transfer path 3-3 shown in Fig. 10A. The other parameters are the same for both the vertical charge transfer paths 3-1 and 3-3. As the signal ST is changed to the positive potential, the charges Q in the vertical charge transfer path 3 are accumulated in the region having the potential P1, as shown in Figs. 9B and 10B.

Next, as the signal C1 is changed to the positive potential, as shown in Fig. 9C the charges Q in the region at the potential P1 move via the region at the potential P2 to the region at the potential P3. As shown in Fig. 10C, in the vertical charge transfer path 3-3, the charges Q in the region at the potential P1 are moved to the regions at the potentials P2 and P3.

Next, the signal C1 is set to 0 V. As shown in Fig. 9D, in the vertical charge transfer path 3-1, the charges Q are stored in the region at the potential P3.

As shown in Fig. 10D, in the vertical charge transfer path 3-3, the charges Q in the regions at the potentials P2 and P3 are returned to the region at the potential P1.

Next, the signal C2 and signal φ1 are changed to the positive potential. As shown in Fig. 9E, in the vertical charge transfer path 3-1, the charges in the region at the potential P3 are moved via the region at the potential P4 to the horizontal charge transfer path 6 at the potential P5. As shown in Fig. 10E, in the vertical charge transfer path 3-3, the charges Q are stored in the vertical charge transfer path 3-3 at the potential P1.

The vertical charge transfer paths 3-2 and 3-4 shown in Fig. 1A correspond to the vertical charge transfer paths 3-1 and 3-3 described above. With this control method described above, the charges only in the vertical charge transfer paths 3-1 and 3-2 can be transferred to the horizontal charge transfer path 6, and the charges in the vertical charge transfer paths 3-3 and 3-4 are not transferred.

Next, a method of transferring the charges in the vertical charge transfer paths 3-3 and 3-4 to the horizontal charge transfer path 6 as described with Fig. 1C will be described with reference to Figs. 11A to 11D.

Fig. 11A is a cross sectional view taken along line X-X' of Fig. 8, similar to Fig. 10A.

In Fig. 11A, the signal ST is set to a positive potential, the signal C1 is set to 0 V, the signal C2 is set to 0 V, and the signal φ1 is set to 0V. Similar to Fig. 10B, as shown in Fig. 11B the potentials at the semiconductor regions under the electrodes 31, 32, 33, 34 and 35a therefore become P1, P2, P3, P4 and P5. As the signal ST is changed to the positive potential, the charges in the vertical charge transfer path 3-3 are accumulated in the region at the potential P1.

As the signal C1 is changed to the positive potential, as shown in Fig. 11C the charges in the region at the potential P1 are moved to the regions at the

potentials P2 and P3.

Next, as the signals C2 and φ1 are changed to a higher positive potential, as shown in Fig. 11D the charges in the regions at the potentials P2 and P3 are moved via the region at the potential P4 to the horizontal charge transfer path 6 at the potential P5.

The vertical charge transfer paths 3-1 and 3-2 operate in a manner similar to the operation of the vertical charge transfer paths 3-3 and 3-4. However, since the charges in the vertical charge transfer paths 3-1 and 3-2 are already transferred and the vertical charge transfer paths 3-1 and 3-2 are empty, the charges only in the vertical charge transfer paths 3-3 and 3-4 are substantially transferred to the horizontal charge transfer path 6.

The p-type region 37 is not necessarily required to be formed in the vertical charge transfer path 3. It is not limited that the same signal C1 is applied to the electrodes 32 and 33 shown in Fig. 8. Instead, a signal C1-1 may be applied to the electrode 32, and a different signal C1-2 may be applied to the electrode 33. In this case, if the signals C1-1 and C1-2 are supplied at different timings, the charges can be transferred more smoothly. If the same signal C1 is applied to the electrodes 32 and 33, a single electrode may be used in common for the electrodes 32 and 33.

In the above embodiment, a solid state image pickup device is used which has photoelectric conversion elements disposed on a two-dimensional plane uniformly in vertical and horizontal directions. A solid state image pickup device of a honeycomb structure to be described below may also be used.

Fig. 12 is a partial plan view of a solid state image pickup device of a honeycomb structure. The solid state image pickup device of a honeycomb structure has a number of photoelectric conversion elements 102 disposed at a constant pitch in a plurality of rows and columns. One photoelectric conversion element column P1

or P2 and one photoelectric conversion element row Q1 or Q2 each have a plurality of photoelectric conversion elements 102. Each of the plurality of photoelectric conversion elements 102 constituting an even column P2 is shifted in the column direction by about a half of the pitch between photoelectric conversion elements in the column, relative to each of the plurality of photoelectric conversion elements 102 constituting the odd column P1. Similarly, each of the plurality of photoelectric conversion elements 102 constituting an even row Q2 is shifted in the row direction by about a half of the pitch between photoelectric conversion elements in the row, relative to each of the plurality of photoelectric conversion elements 102 constituting the even row Q1. Each of the photoelectric conversion element columns P1 and P2 includes only the photoelectric conversion elements of either the odd row Q1 or the even row Q2.

In order to transfer red (R), green (G) and blue (B) pixel charges accumulated in the photoelectric conversion elements, a plurality of vertical charge transfer paths 103-1 to 103-6 are formed each between the odd column pixels 102 (R, G, R, G,...) and the even column pixels 102 (G, B, G, B,...). Each vertical charge transfer path 103 is disposed in a zigzag way to transfer signal charges along a predetermined direction (to a downstream side).

Each vertical charge transfer path 103 has a plurality of transfer electrodes 111-1 to 111-9. The plurality of transfer electrodes 111 are disposed in a honeycomb shape. Each photoelectric conversion element is disposed in plan in each of hexagonal spaces defined by disposing the plurality of transfer electrode 111 in a honeycomb shape.

The horizontal charge transfer path 106 is made of CCDs, receives electric charges of one row unit transfers charges from the left area of the drawings of Fig. 12 to the right area (in a horizontal direction).

The output amplifier 107 outputs a voltage corresponding to the amount of charges transferred from the horizontal charge transfer path 106.

Control electrodes 105 control the read (transfer) operation of electric charges from the vertical charge transfer path 103 to the horizontal charge transfer path 106.

The charge addition in the vertical and horizontal directions for the solid state image pickup device of this structure can be performed by a control method same as that used for the solid state image pickup device described with Fig. 1A. For example, as a read pulse is applied to the transfer electrode 111-2, charge signals R, G, R, G,... are read to the vertical charge transfer path 103 disposed in the horizontal direction and transferred to the vertical charge transfer path 103 under the transfer electrode 111-6. As a read pulse is applied to the transfer electrode 111-6, addition signals RR, GG, RR, GG of two pixels can be obtained. Addition signals GG, BB, GG and BB of two pixels under the transfer electrode 111-8 can be obtained in a similar manner. The signal charge transfer and addition of pixels in the horizontal charge transfer path to be executed thereafter are similar to the operation described with Fig. 1A.

The present invention has been described in connection with the preferred embodiments. The invention is not limited only to the above embodiments. It is apparent that various modifications, improvements, combinations, and the like can be made by those skilled in the art.